

Lead/Senior Digital Design Engineer

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Company: Cyient

Location: Leuven

Category: computer-and-mathematical

Description

Do you have a passion for building entirely new solutions? As part of our Digital Design team, you'll take imaginative ideas and turn them into reality.

Responsibilities

Architecture/Micro-architecture specification development

RTL implementation using VHDL or Verilog/System Verilog

Lint, clock domain crossing (CDC) analysis, top level integration, Synthesis, & Power Optimization

Collaboration with verification team on planning and execution, simulation, debugging block and system level simulations, formal verification, preparation of technical reviews and product/block documentation

Collaboration with the backend team to analysis and optimize the design in terms of timing, area and power

Soft and hard 3rd party IP identification, selection and integration

Contribute to flow and methodology development

This a position that requires leading a team

Minimum Qualification

Bachelor's or Master's Degree in Electrical or Computer Engineering

6+ years of relevant digital design experience

Strong communication, presentation and team leading skills

Strong understanding of ASIC design flow

Strong Experience with RTL coding in VHDL and/or Verilog/System Verilog

Strong Experience with EDA tools (simulation, synthesis, logic equivalency check, static timing analysis and power analysis)

Experience with scripting languages (TCL, Python, Perl, Shell-scripting)

Experience in CPU, Memory and Peripheral Subsystems

Preferred Qualification

Knowledge of mixed signal concepts

Functional Verification experience or understanding (assertion based verification, code coverage, functional coverage, test plans, UVM, etc.)

Experience with basic C/C++ programming

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Skills & Experience

Application-Specific Integrated Circuit (ASIC) Development, RTL Coding, SystemVerilog

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